

# VERIFICATION OF TRMS WITH IP COMPONENT DESIGN

**K.SIEKIERSKA, A.KOKOSZKA, D.OBRĘBSKI, N.ŁUGOWSKI  
P. FRAŚ\*, T. KOSTIENKO\*, A.PAWLAK\*, P. PENKALA\*,  
D. STACHAŃCZYK\*, M. SZLĘZAK\***

INSTITUTE OF ELECTRON TECHNOLOGY, WARSZAWA, POLAND

\*SILESIA UNIVERSITY OF TECHNOLOGY, GLIWICE, POLAND

**KEYWORDS: COLLABORATIVE ENGINEERING, IP COMPONENTS**

**ABSTRACT:** The paper presents a new system for management of dispersed tools that enables realization of distributed design workflows. The Tool Registration and Management System (TRMS) has been verified by its deployment to a process of IP component design. The possibility of agile and transparent use of remote design tools is its greatest advantage from the IP provider point of view. A friendly GUI helps a designer in definition of design workflows that integrate distributed tools. TRMS supports collaborative design style in the Internet space.

## INTRODUCTION

Collaborative engineering is one of the new technologies for efficient product development that allows integration of widely distributed engineers. This network-based computer-supported cooperative work (CSCW) paradigm is still a young field of research and development aiming at increase of design productivity required by current IP-based SoC designs. The main problem in network-based design relates to obstacles created by firewalls, but easy tool integration, format conformities, standards usage etc. should be also resolved.

The Advanced Collaborative Infrastructure (ACI), developed in the frame of the E-Colleg project [4] allows to integrate remote tools and cross firewalls transparently. Advanced Network Transport Services (ANTS) [3] are a set of services providing secure site-to-site transport of data using the network infrastructure. ANTS are used by TRMS to perform data transmission overcoming firewalls. The system has been developed on the Java platform with commonly available technologies and tools like UML, XML, SQL and Web. There were some GUIs developed basing on the TRMS [4], but the one based on TRMS-GTLS (Global Tool Look-up Service) is much more advanced [5]. The last environment is closer to designers' needs having e.g. the virtue of much more easier tools integration comparing with the previously presented one. ITE and SUT were testing the TRMS-GTLS with IP component design.

The paper is organized as follows: firstly, the methodology of collaborative SoC design with emphasis on IP components design is discussed, secondly, the short description of TRMS features and services are addressed, next IP design dedicated workflows are shown and finally short conclusions are presented.

## METHODOLOGY FOR COLLABORATIVE DESIGN

The term *collaborative design* is usually used with regard to realisation of complex design or SoC performed by the geographically dispersed group of engineers. This scenario of work is quite common nowadays, for example when the large design company, to decrease system design cost, commissions small enterprise (SME) to develop selected system components. The Internet is a medium that can significantly improve the collaboration in such distributed design environment. The development of current complex digital circuits requires close cooperation between engineers responsible for all stages of design. The collaborative design methodology should provide the mechanisms supporting work of IP designers as well as engineer responsible for integration of final project. From the IP component designer point of view the most important is an easy access to design data and tools. In a case of a SME that can hardly ever afford for expensive design tools the remote use of provided by cooperating company tools is essential advantage. The very important issue is an intellectual property (IP) protection, the collaboration platform has to provide the mechanisms for secure tool invocation and data exchange between partners' networks protected by firewalls.

In this paper the advantages of a collaborative design for IP designers will be discussed. The key issue related to possibility of applying remote tools owned by some partners by any other partner, have been partially resolved by the tools developed under E-Colleg project: Visual S3S Client GUI [4] and TRMS-GTLS [6]. The last tool was used to establish collaborative design environment, presented below.

## COLLABORATIVE IP DESIGN SCENARIO

In this paper we limit our discussion to the part of collaborative work related to digital components design by site-dispersed designers. The design methodology, based on HDL (VHDL or Verilog) and RTL synthesis, is generally the same as in the case of on-site design [7], but some processes are performed using remote tools. Collaborative IP component design is shown

schematically in fig. 1. There are two or three tools respectively to target implementation (standard cell ASIC or FPGA), which should be shared. Synthesis and simulation tools are remotely used in both cases, but the post-synthesis simulation is performed in the case of an ASIC target technology and the post-implementation simulation is performed in the case of an FPGA. The last one has to be preceded by remote implementation and generation of needed files.

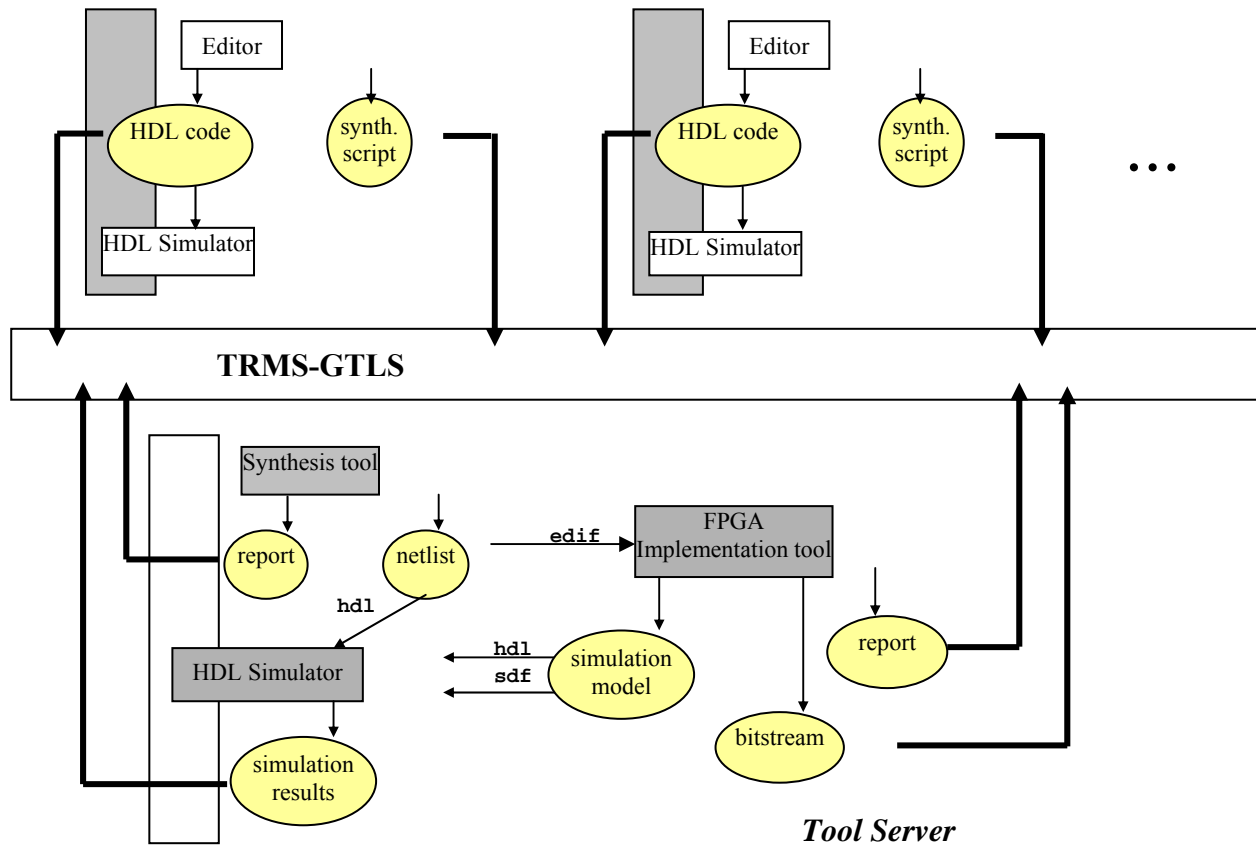


Fig. 1. Schematic of collaborative IP component design

**Local simulation.** Each designer should have at his disposal an HDL simulator (*Client server1/2* in fig. 1) to use it locally, because a graphical output of simulation can't be sent by network in practice. There is a lot of HDL simulators in the market and the cost of some of them is not too high (even there are some GNU-license based free simulators on the Linux platform). Analysis of simulation results basing only on the text format information (like signal values snapshots), which can be easily interchanged by a network, is very uncomfortable in a real design, especially in the early phase of design, when the architecture of the component is often changed. A designer has to view waveforms in debugging phase of a new developed HDL code to verify their correctness.

Text simulation results are usually generated for the final verified version of the component to be compared with simulation results of a related post-synthesis structure, which can be performed remotely.

**Remote synthesis and simulation.** A synthesis tool cost is much higher than a simulator cost, then it is reasonable to share the tool in a network (accomplishing the license agreement) among the partners that have not got their own one. They can perform synthesis of a developed component on the remote machine (*Tool server* in fig. 1) to check if the code is synthesisable and choose the best optimisation conditions. Data transfer in both sides can be restricted to sending HDL models and a synthesis script in one direction and resending synthesis report in the other one. Simulation of the post-synthesis netlist has to be performed remotely, because simulation models of all standard cells from the used standard cell ASIC library are a part of Design Kit located at the synthesis tool owner's site. Simulation results in the text format can be easily compared with the final simulation results of the HDL component source code.

**Remote implementation and simulation.** The final design phase in the case of FPGA – mapping, placement&routing and generation of back-annotated files for simulation and a bit-stream file for implementation into a selected device - can be also performed remotely. Designer can validate his IP component in a way of post-implementation simulation (*Tool Server* in fig. 1) to compare the results with the related HDL source code. The implementation report gives designer a valuable information about timing and area parameters of the developed IP.

## TOOL REGISTRATION AND MANAGEMENT SYSTEM

TRMS [2][3][4] is an environment for remote tools invocation, which assures secure transmission of data generated by the invoked tools as well as the management of user rights to access specific tools. It includes support for transformation and registration of new tool definitions. TRMS uses the native XML database for storing tool definitions. It provides a very efficient way to exchange information between and within organizations that support this standard. The TRMS client is a powerful Windows-based GUI that allows efficient, user friendly management of tools and users registered in the environment. Through that it supports a designer to search for establishing a distributed design environment to solve a particular design problem. A designer doesn't waste time to write long tool configuration scripts. Instead, he can login through the TRMS client to the system in order to find required tools. In the next step he can build a workflow that suits his particular design task.

TRMS does not restrict a user to a particular design methodology. Instead, one can deploy the best available tools for solving one's design problem following the most appropriated design methodology. Configuration of a distributed design environment is highly reusable, as all information and design configuration are being stored as XML-files.

TRMS is an engineering domain transparent, i.e. tools might come from various engineering domains.

The paper describes how end-user, e.g. an IP designer can use TRMS for improving the design process with his workflow that integrates the registered and selected tools.

## TRMS USAGE

First off all, each designer must be registered in GTLS by the TRMS administrator, as well as he must generate the keys for authorization. After that he can login into the environment and look for interesting tools using name or keyword criteria (e.g. he can use the keyword "implementation" in the case of Xilinx tools).

## Tools

Designer gets the list of tools with their names, short descriptions and related keywords. The tool server name and its current availability for invocation of each tool is

listed, too. The additional information concerning the selected tool, like: a version number, description, available parameters, inputs and outputs, the IP address of the tool server can be viewed. If the tool features satisfy the design requirements, the tool can be parameterized (by choosing the options and arguments, redefining input/output) and invoked separately, or included into the design workflow.

## Workflows

When designer knows which tools he needs, and these tools should be invoked sequentially, the best way of using them is their integration into the workflow. Creation of the workflow is very easy in the TRMS-GTLS. A designer simply chooses particular tools and parameterizes them in the same way as in the separate use described above. He must only remember about matching of the inputs of the following tool with the outputs of the preceding one. The tools in the workflow can be invoked manually or automatically one by one, what accelerates the design process. Once created workflow can be exported to the XML file and reused in a different application.

## IP component design workflow

Collaborative IP design schematically shown in fig. 1 was implemented into two TRMS workflows – for ASIC and FPGA design.

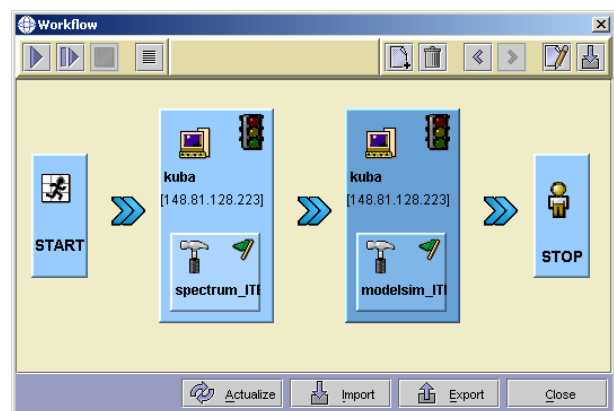


Fig.2 ASIC design workflow

The first one (fig. 2) is relatively simple, it contains two tasks only: synthesis and post-synthesis simulation. For that tasks Leonardo Spectrum and Modelsim tools (both in command line mode) were used respectively.

In the case of the FPGA workflow, the implementation process (fig. 3) must be additionally included. This process consists of five tasks: ngdbuid, map, par, netgen, bitgen (parts of Xilinx ISE). Each of them (excluding the first one) needs as its input the output of the previous one, and there is no need for human interaction, so the automated invocation is very useful in this case. If some of the tools return the exit code different than "0" the workflow is stopped, additionally each of the tools generates a report which is sent to the designer, therefore all the time IP designer can monitor the progress and status of the workflow performance.



Fig. 3 Implementation part of FPGA design workflow

## CONCLUSIONS

Remote synthesis and FPGA implementation services could be very attractive not only in collaborative design but also for IP providers or generally SMEs to support their own designs without having own synthesis and implementation tools.

IP components developed locally must be validated basing on the synthesis tools and the result netlist simulation. An IP provider attains such a possibility due to the TRMS-GTLS environment. On the other hand, a final product engineer supported by the environment is able to convert his own design idea into a working hardware prototype on the application board using FPGAs configured by EEPROMs supplied by bit stream files generated as an output of the remote workflow.

TRMS is still in the evaluation phase. Nevertheless, its current functionality is already very useful for an IP designer. Easy search and integration of required tools allow for the design productivity improvements. Workflow-centred design process seems to be a very attractive design paradigm for designers, as it allows them to concentrate on the main challenges of a design leaving integration of tools to the described TRMS environment.

Before the TRMS-based distributed work paradigm could be fully exploited a number of open issues need to be resolved, like: e-commerce issues related to remote tool usage, distributed licence management, etc. Further work includes also more powerful design workflow management system that is central to efficient usage of distributed resources.

**Acknowledgments** - The work described herein has been founded by the IST project E-Colleg (IST-1999-11746) and supported additionally by KBN SPB grants.

## THE AUTHORS

Dr Krystyna Siekierska, Artur Kokoszka, Dariusz Obrębski and Norbert Ługowski are with the ICs and Systems Design Dept. of Institute of Electron Technology, Al.Lotników 32/46, Warszawa, Poland e-mail: {k.siek, kokoszka, obrebski, lugowski}@ite.waw.pl

Dr Adam Pawlak, Paweł Fraś, Piotr Penkala, Darek Stachańczyk and Marek Szlęzak are with Silesian Univ. of Technology. Tomasz Kostienko was enrolled in Ph.D. studies at SUT.

## REFERENCES

- [1] Kokoszka A., Ługowski N., Nguyem Q. T., Obrębski D., Pawlak A., Siekierska K., Carbellada M., Schlichter B.: "Collaborative Design of the FWMI (FPGA Pulse Width Modulator Industrialized Version)", Proc. of E-Colleg Workshop on Challenges in Collaborative Engineering (CCE'03), Poznań, 15-16 April 2003.
- [2] T. Kostienko, W. Mueller, A. Pawlak, T. Schattkowsky, Advanced Infrastructure for Collaborative Engineering in Electronic Design Automation, 10th ISPE Int. Conf. on Concurrent Engineering: Research and Applications, Madeira Island, Portugal, 26-30.07.2003.
- [3] Tim Schatkowsky, Wolfgang Mueller: "Distributed Engineering Environment for the Design of Electronic Systems", Proc. of CCE'03, Poznań, Poland, 15-16 April 2003.
- [4] E-Colleg project web page <http://www.ecolleg.org>
- [5] K.Siekierska, D.Obrębski, A.Kokoszka, N.Ługowski, A.Pawlak, M.Carballada, B.Schlichter: "Verification of Advanced Collaborative Infrastructure by Affine FPGA Design, Workshop on Challenges in Collaborative Engineering", CCE'04, Tatranska Lomnica, Slovakia, April 18-21, 2004
- [6] Tomasz Kostienko, Adam Pawlak, Marek Szlęzak, Paweł Fraś, Jarosław Magiera, Maciej Witczyński: "Development of TRMS/GTLS – Global Tool Lookup Services", Proc. of CCE'03, Poznań, Poland, April 15-16, 2003.
- [7] Kokoszka A., Nguyen Q.T., Siekierska K., Pawlak A., Obrębski D., Ługowski N.: "Distributed Design of Semiconductor IP Based on the Workflow Concept", Proc. of IEEE Design and Diagnostic of Electronic Circuits and Systems Workshop, IEEE DDECS 2001, Gyor, 18-20 April, 2001, pp. 299-306.
- [8] IEEE Std 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture